REMARKS

The foregoing Amendment and remarks which follow are responsive to the Office Action mailed May 16, 2003 in relation to the above-identified patent application. In that Office Action, the Examiner rejected Claims 1-7 and 17-26 under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent No. 10-22447, and rejected Claims 1-7 and 17-26 under 35 U.S.C. § 102(e) as being anticipated by the Combs et al. reference. Additionally, the Examiner rejected Claims 1-7 and 17-26 as being unpatentable over the combination of the Gow et al. and Casto et al. references.

By this Amendment, Applicant has amended independent Claim 17 to describe the chip mounting pad of the leadframe as defining a peripheral edge, and the isolated ring structure as extending between the peripheral edge of the chip mounting pad and the inner ends of the leads in spaced relation thereto.

Applicant respectfully submits that independent Claims 1 and 23 in their originally presented format and the amended version of independent Claim 17 are not anticipated by the cited Japanese reference. In each of independent Claims 1 and 17, the isolated ring structure is described as being disposed between the peripheral edge of the chip mounting pad and the inner ends of the leads. Similarly, in independent Claim 23, the means for allowing two of the input/output pads of the semiconductor chip to be electrically connected to a common one of the leads is described as being disposed between the peripheral edge of the chip mounting pad and the inner ends of the leads.

Applicant respectfully submits that the orientation of the ring structure between the peripheral edge of the chip mounting pad and the inner ends of the lead is not taught, suggested, or shown in any one of Figures 1-9 of the cited Japanese reference. As is best shown in Figures 5-9 of the Japanese reference, the semiconductor device shown and described therein comprises a square heat sink which defines a generally planar top surface. Attached to the top surface of the heat sink is a square piece of insulating tape which has a square opening formed in the approximate center thereof. As is seen in Figure 9, the outer peripheral edge of the insulating tape extends to a point just inward of the outer peripheral edge of the heat sink. Disposed within the central opening defined by the insulating tape is a semiconductor die which is placed directly upon the top surface of the heat sink. Disposed

on the top surface of the insulating tape is a lead frame which includes first and second rings and a plurality of elongate leads. The first and second rings are disposed upon the insulating tape, as are the inner portions of each of the leads. The semiconductor die is electrically connected to the top surfaces of the first and second rings and the top surfaces of the leads through the use of conductive wires. The semiconductor die, conductive wires, first and second rings, leads, insulating tape and heat sink are covered by a package body such that the bottom surface of the heat sink is exposed in the bottom surface of the package body, and the outer portions of the leads protrude from respective side surfaces of the package body.

Applicant respectfully submits that in the cited Japanese reference, the structural element which is analogous to the chip mounting pad recited in each of independent Claims 1, 17 and 23 is the heat sink. However, the first and second rings described in the Japanese reference clearly do not extend between the peripheral edge of the heat sink and the inner ends of the leads. Rather, as explained above and is most clearly shown in Figure 9 of the Japanese reference, the first and second rings are disposed on the insulating tape layer between the inner ends of the leads and the side surfaces of the semiconductor die. Indeed, both the first and second rings and the inner portions of the leads which are all disposed upon the insulating tape layer are located well inward of the outer peripheral edge of the heat sink. Thus, Applicant respectfully submits that independent Claims 1, 17 and 23 are not anticipated by the Japanese reference due to the recitation in such claims of the ring structure (in the case of Claims 1 and 17) or the means (in the case of Claim 23) being described as extending between the peripheral edge of the chip mounting pad and the inner ends of the leads.

Additionally, Applicant notes that the limitations recited in certain ones of the dependent claims of the present application are not satisfied by the teachings of the cited Japanese reference. For example, in Claims 2 and 18, the inner end of each of the leads is described as being vertically downset from the distal end thereof (in the case of Claim 2) or from the chip mounting pad (in the case of Claim 18) at a distance approximately equal to the lead thickness. As best seen in Figure 9 of the Japanese reference, the downset of the inner end of each of the leads relative to the distal end thereof or to the heat sink clearly exceeds the thickness of such lead. Additionally, in each of Claims 3 and 26, the top surface of the

inner end of each of the leads is described as being aligned with the top surface of the semiconductor chip. As is also clearly shown in Figure 9 of the cited Japanese reference, such alignment is clearly not present in the semiconductor device disclosed therein in that the top surfaces of the inner ends of the lead are disposed well below the top surface of the semiconductor die.

Applicant respectfully submits that independent Claims 1, 7 and 23 are also not anticipated by the Combs et al. reference due to such reference also lacking any teaching or suggestion regarding the orientation of a ring between the peripheral edge of the chip mounting pad and the inner ends of the leads. In the various embodiments of the integrated circuit package shown and described in the Combs et al. reference, both the semiconductor die 102 and the interposer ring 103 are attached to a common surface of the heat sink 104, the semiconductor die 102 being electrically connected to both the ring 103 and the inner portions of the leads 109 of the package through the use of bond wires 110. Thus, Applicant respectfully submits that the Combs et al. reference also fails to teach or suggest the ring 103 extending between the peripheral edge of the heat sink 104 and the inner ends of the leads 109 as is recited in relation to the ring in independent Claims 1 and 17 and the means in independent Claim 23.

Applicant further notes that the limitations recited in certain ones of the pending dependent claims of the present application are not satisfied by the cited Combs et al. reference. More particularly, Applicant respectfully submits that the Combs et al. reference fails to teach, suggest or show the top surfaces of the inner ends of the leads 109 being aligned with the top surface of the ring 103 (Claims 4, 19, and 25) or the inner end of each of the leads 109 being downset relative to the distal end thereof a distance approximately equal to the lead thickness (Claim 2) or downset from the heat sink 104 a distance approximately equal to the lead thickness (Claim 18).

The deficiencies of the cited Japanese and Combs et al. references discussed above also hold true in relation to the Gow et al. reference cited as the primary reference in support of the Section 103(a) rejection. As is best seen in Figures 2-4 of the Gow et al. reference, a semiconductor chip 10 is mounted to the top surface of a chip bond pad portion 13 of a lead frame 12. The lead frame 12 also includes a plurality of lead fingers 16, 18 which extend

toward the pad portion 13 in spaced relation thereto. Extending along the top surfaces of the lead fingers 16, 18 is a pier 24 which is fabricated from a plastic material and includes multiple metal pads 26 disposed from the top surface thereof in spaced relation to each other. The chip 10 attached to the top surface of the pad portion 13 is electrically connected to the pads 26 and to the top surfaces of the lead fingers 16, 18 through the use of wires 20, 27. As is apparent from the foregoing, the pier 24 in the Gow et al. reference does not extend between the peripheral edge of the pad portion 10 and the inner ends of the lead fingers 16, 18, but rather extends along the top surfaces of the lead fingers 16, 18. Thus, Applicant respectfully submits that independent Claims 1, 17 and 23 are not rendered obvious by the combination of the Gow et al. and Casto references, the Casto reference being devoid of any teaching or suggestion regarding a ring structure. Additionally, Applicant respectfully submits that the Gow et al. reference fails to teach or suggest the top surfaces of the inner ends of the lead fingers 16, 18 being aligned with the top surface of the pier 24 in accordance with Claims 4, 19, and 25 since such relationship is not possible due to the extension of the pier 24 directly along the top surfaces of the lead fingers 16, 18.

On the basis of the foregoing, Applicant respectfully submits that the stated grounds of rejection have been overcome, and that Claims 1-7 and 17-26 are now in condition for allowance. An early Notice of Allowance is therefore respectfully requested.

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

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